REMARKS

Applicant has reviewed the Office Action mailed on June 18, 2003, as well as the art cited. Claims 1-31 are pending in this application. Application has proposed amending claims 25 and 28 as directed in the Office Action. It is respectfully requested that these proposed amendments be entered.

Information Disclosure Statement

Applicant respectfully requests that a copy of the 1449 form, listing all references that were submitted with the Information Disclosure Statement filed on July 3, 2001, marked as being considered and initialed by the Examiner, be returned with the next official communication.

Claim Objections

Claim 25 was objected to because claim 25 recites a "pair of amplifier input" when it should be a "pair of amplifier inputs". Applicant respectfully requests that the proposed amendment to claim 25 making this correction be entered.

Rejections Under 35 U.S.C. § 112

Claims 8-14 and 23-31 were rejected under 35 USC § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the Applicant regards as the invention.

The Office Action rejected claims 8 and 23 since those claims recite an "input signal" and do not specify "first, second, or some other input signal."

Applicant respectfully requests reconsideration of this rejection. It is respectfully submitted that the recitation of "an input signal" in claim 8 of the present application is not indefinite. In relevant part, claim 8 of the present application recites "a differential phase detector that receives *an input signal* and a feedback *signal* and produces a differential output *signal*", "at least one first *input* coupled to the differential output *signal* of the phase detector",

"a second *input* that is responsive to a detected state of the input *signal*", and "at least one *amplifier input*, wherein the electronic selector circuit provides the differential output *signal* of the phase detector to the amplifier *input*." It is respectfully submitted that there is no confusion between the recitation of an input and a signal. Accordingly, Applicant respectfully requests that this rejection be withdrawn.

Claims 9-14 were rejected because they depend from claim 8. Claim 23 was rejected for the same reason as claim 8. Claims 24-31 were rejected because they depend from claim 23. It is respectfully requested the rejection of these claims be withdrawn for the same reason set forth above with respect to claim 8.

Claim 28 was rejected because that claim recited "the method of claim 28", which lacks antecedent basis. The proposed amendment to claim 28 corrects this informality with claim 28. Applicant respectfully requests that this amendment be entered and that this rejection be withdrawn.

Rejections Under 35 U.S.C. § 102

Claims 1, 2, 3, 8, 10, 14, 23, 24, 26, and 30 were rejected under 35 USC § 102(b) as being anticipated by Abe et al. (U.S. Patent No. 5,319,320) (referred to here as "Abe").

Applicant respectfully requests reconsideration of this rejection. Claim 1 is directed to a "phase locked loop circuit" that recites, in relevant part, "a differential phase detector that receives *an input signal* and *a feedback signal* and produces a differential output signal" and "wherein the electronic selector circuit is operable to control the amplifier input *to hold the output frequency of the voltage controlled oscillator* at a substantially constant frequency *when the input signal to the phase detector is interrupted*."

The Office Action cites paragraphs 5 and 6 of Abe in making this rejection. The following portion of paragraphs 5 and 6 of Abe are cited in the Office Action:

> Since oscillation frequency f.sub.OSC of voltage-controlled oscillator 40 is varied by the value of the filter output voltage V.sub.F, the phase difference between oscillator output V.sub.OUT and input signal S.sub.IN becomes zero as time progresses.

> During a time in which signals X.sub.1, X.sub.2 of each period are not generated, an integrated load is stored in capacitor C.sub.F, and, therefore, the output of voltage-controlled oscillator 40 is controlled by that charging voltage. Therefore, the charging voltage of capacitor C.sub.F for current i functions as a frequency control signal for the pull-in operation that matches oscillation frequency f.sub.OSC to the frequency of input signal S.sub.IN.

Abe, column 1, line 62 – column 2, line 1. The Office Action goes on to reason that "when the output of VCO is 0, at least one input of the phase comparator, element 60 in fig 1, is interrupted." Thus, the Office Action is taking the position that it is the output of the VCO (item 50 in FIG. 1 and item 40 in FIG. 4) that is interrupted.

As an initial matter, the cited paragraphs 5 and 6 of Abe relate to FIG. 4 of Abe, not FIG. 1. Thus, it is respectfully submitted that the cited paragraphs 5 and 6 of Abe are not describing the operation of the circuit shown in FIG. 1 and reliance thereupon for describing the operation of the circuit shown in FIG. 1 of Abe is inappropriate.

Moreover, it is respectfully submitted that the output of the VCO 50 of Abe cannot properly be considered "the input signal" recited in claim 1 of the present application. As noted above, claim 1 recites "a differential phase detector that receives *an input signal* and *a feedback signal*." In other words, in the context of claim 1 of the present application, there is a distinction between "the input signal" received by the differential phase detector and "the feedback signal" received by the differential phase detector. The output of the VCO 50 of Abe is a "feedback signal" received by the phase comparator 60 of Abe. It is not an "input signal" as that term is used in the context of claim 1 of the present application. In fact, this same distinction is made in Abe: "A phase-locked loop 100 comprises a digital phase comparator (PC) 60 which compares the phase of an *input signal* S_{IN}, as a reference signal, with the phase of an *output* V_{OUT} (at oscillation frequency f_{OSC}) of *a voltage-controlled oscillator 50. . . .*" Abe, column 5, line 66 – column 6, line 3. See also, for example, claim 1 of Abe ("A phase-locked loop that detects the phase difference between *an input signal*, which is a reference signal, and *an oscillator output.*"). Therefore, regardless of whether or not the output of VCO 50 is interrupted, the output of VCO 50 cannot properly be considered "an input signal" (as opposed to "a feedback signal") as recited

in claim 1 of the present application. Accordingly, Abe does not teach or suggest "wherein the electronic selector circuit is operable to control the amplifier input to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency *when the input signal to the phase detector is interrupted.*"

In response to the arguments made in Applicant's previous Amendment and Response, the Office Action stated that "As per constant frequency and interrupted signal, this can occur in a number of ways. Based on paragraphs 5 and 6, interrupted signal is shown in a number of ways such as capacitor can be discharged, voltage difference can be 0, output of VCO can be 0 which would interrupt the input into phase element 60 in fig. 1. Also, fig. 3 shows lines indicating 0 current, or 0 voltage or L data which are also interrupted signals and these lines during interruptions are constant and thus at a constant frequency. Figure 3 also shows such constant lines for different amounts of time which also indicated signal interruption. This is also valid for figure 6."

Applicant respectfully submits that the capacitors of Abe (the ones in filter 75 of FIG. 1 or C_F in FIG. 4) in no way interrupt "an input signal" (as that term is used in claim 1) received by a differential phase detector nor produce "the output frequency of the voltage controlled oscillator" as recited in claim 1 of the present application. For example, the output of the filter 75 is not the output of VCO 50 nor is it used as an input signal to the phase comparator 60 of Abe. Instead, the output of filter 75 is used as an input to the buffer circuit 91 of Abe. Similarly, the output capacitor C_F of FIG. 4 is not the output of VCO 40 nor is it used as an input signal to the phase comparator 10 shown in FIG. 4 of Abe. Thus, any interruption of the output of these capacitors would not be an interruption to "an input signal" received by a differential phase detector as recited in claim 1 of the present application. Moreover, the output of these capacitors is not "the output frequency of the voltage controlled oscillator" as recited in claim 1 of the present application.

As to the output of VCO 50 of Abe, Applicant respectfully submits that the output of VCO 50 cannot properly be considered "an input signal" as recited in claim 1 of the present application for the reasons set forth above. Thus, any interruption of the output of VCO 50 is not an interruption to an input signal of phase comparator 60.

Furthermore, the lines shown in FIG. 3 of Abe do not correspond to "an input signal" received by a differential phase detector as recited in claim 1 of the present application. Also, the lines shown in FIG. 3 of Abe do not correspond to "the output frequency of the voltage controlled oscillator" as recited in claim 1 of the present application. The signals X_1 and X_2 are "phase error signals" *output* by phase comparator 60 of Abe. The signal i_1 is the output current of first charge pump 70. The signal V_1 is a voltage at a series connection point P_1 of capacitors C_1 and C_2. The signal i_3 is the current flowing through resistors R_1 or R_2. The signal i_2 is the output current of second charge pump 80. The signal i_4 is the current that flows from addition point P_2 to the output terminal side of operational amplifier 92 through return resistor R_3. The signal V_2 is the input voltage of VCO 50. None of the signals shown in FIG. 3 of Abe are an input signal received by phase comparator 60. None of these signals are outputs of VCO 50. Even if one or more of these signals influence the output of the VCO 50 (or even somehow interrupt the output of VCO 50), the output of the VCO 50, as explained above, is not "an input signal" (as opposed to a feedback signal) as recited in claim 1 of the present application. Therefore, none of the lines shown in FIG. 3 of Abe correspond to "an input signal" received by a differential phase detector or "the output frequency of the voltage controlled oscillator" as recited in claim 1 of the present application.

Based on the foregoing, it is respectfully requested that this rejection of claim 1 of the present application be withdrawn.

Claims 2 and 3 of the present application depend from claim 1. Therefore, based on the arguments set forth above with respect to claim 1, it is respectfully requested that the rejection of claims 2 and 3 of the present application be withdrawn.

Claim 8 of the present application is directed to a phase locked loop circuit. In relevant part, claim recites "a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal" and "wherein the electronic selector circuit de-couples the amplifier input from the differential output *and* holds the output frequency of the

voltage controlled oscillator to a last received signal from the differential output *when the input signal to the phase detector is interrupted.*"

The Office Action took the position that "in fig. 1 if R1 is much larger than R2 or vice versa, then this equates to decoupling both outputs of the phase detector which are narrowed to just one input into the switch." Even if this is true (which Applicant does not concede), there is no explanation as to how Abe teaches that this decoupling occurs when the input signal to the phase detector is interrupted as recited in claim 8. The Office Action also cites paragraphs 5 and 6 of Abe to support its contention that Abe teaches this. As noted above, paragraphs 5 and 6 of Abe do not provide any teaching relating to when the *input signal* to the phase detector is interrupted. Moreover, as noted above, paragraphs 5 and 6 of Abe relate to FIG. 4 of Abe, which does not include resistors R1 and R2. It is respectfully submitted that the cited paragraphs 5 and 6 are not describing the operation of the circuit shown in FIG. 1 of Abe, which the Office Action relies on in rejecting claim 8.

Based on the foregoing, it is respectfully requested that this rejection of claim 8 of the present application be withdrawn.

Claims 10 and 14 of the present application depend from claim 8. Therefore, based on the arguments set forth above with respect to claim 8, it is respectfully requested that the rejection of claims 10 and 14 of the present application be withdrawn.

Claim 23 is directed to a method for preventing data errors in a communication system. Claim 23 recites, in relevant part, "wherein the phase locked loop includes: a differential phase detector that receives an input signal and a feedback signal and produces a differential output signal" and "using the electronic selector circuit to control the amplifier input to to hold the output frequency of the voltage controlled oscillator at a substantially constant frequency when the input signal to the phase detector is interrupted."

The Office Action rejected claim 23 apparently for the same reasons set forth above with respect to claims 1 and 8.

Based on the arguments set forth above with respect to claims 1 and 8, Applicant respectfully requests that this rejection be withdrawn.

Claims 24, 26, and 30 of the present application depend from claim 23. Therefore, based on the arguments set forth above with respect to claim 23, it is respectfully requested that the rejection of claims 24, 26, and 30 of the present application be withdrawn.

Rejections Under 35 U.S.C. § 103

Claims 11, 12, 27, and 28 were rejected under 35 USC § 103(a) as being unpatentable over Abe et al. (U.S. Patent No. 5,319,320) in view of Satoshi (JP 56051140).

Claim 31 was rejected under 35 USC § 103(a) as being unpatentable over Abe et al. (U.S. Patent No. 5,319,320).

Claims 11 and 12 depend from claim 8. Therefore, based on the arguments set forth above with respect to claim 8 above, it is respectfully requested that this rejection of claims 11 and 12 be withdrawn.

Claims 27, 28, and 31 depend from claim 23. Therefore, based on the arguments set forth above with respect to claim 23 above, it is respectfully requested that the rejection of claims 27 and 28 and the rejection of claim 31 be withdrawn.

Allowable Subject Matter

Claims 15 and 16-22 were allowed.

Claims 4, 5, and 6 were objected to as being dependent upon a rejected base claim, but were indicated to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 7, 9, 13, and 29 were indicated to be allowable if rewritten to overcome the rejection(s) under 35 USC § 112 set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

Claim 25 was indicated to be allowable if rewritten to overcome the rejection(s) under 35 USC § 112 set forth in the Office Action and to include all of the limitations of the base claim and any intervening claims.

CONCLUSION

Applicant respectfully submits that the claims 1-31 are in condition for allowance and notification to that effect is earnestly requested. If necessary, please charge any additional fees or credit overpayments to Deposit Account No. 502432.

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 332-4720.

Respectfully submitted,

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